What is claimed is:

1. A method of manufacturing a SONOS memory, the method comprising:

forming a silicon oxide-silicon nitride-silicon oxide (ONO) dielectric layer on a substrate;

forming a buffer layer on the ONO dielectric layer, the buffer layer having a trench exposing a portion of the surface of the ONO dielectric layer;

forming first conductive spacers on inner walls of the trench;

separating the ONO dielectric layer into two portions by selectively removing the exposed portion of the ONO dielectric layer using the first conductive spacers as an etch mask;

forming a gate dielectric layer on the exposed substrate resulting from the separation of the ONO dielectric layer, the gate dielectric layer extended onto exposed sidewalls of the separated ONO dielectric layer and the first conductive spacers inside the trench and also onto top surface of the buffer layer;

forming a second conductive layer on the gate dielectric layer to fill a gap between the inner walls of the trench;

removing the gate dielectric layer exposed by the second conductive layer;

removing the buffer layer using the first conductive spacers as an etch mask; and

patterning the two-separated ONO dielectric layers by selectively removing a portion of each of the separated ONO dielectric layer, which is exposed by the removal of the buffer layer, using the first conductive spacers as an etch mask.

2. The method as claimed in claim 1, wherein the gate dielectric layer is formed of silicon oxide using thermal oxidation or chemical vapor deposition.

3. The method as claimed in claim 1, wherein forming the second conductive layer comprises:

depositing the second conductive layer on the gate dielectric layer to fill a gap between inner walls of the trench completely; and

exposing a portion of the gate dielectric layer, which is extended onto the buffer layer, by etching the second conductive layer using an etchback process or chemical mechanical polishing or both.

4. The method as claimed in claim 3, wherein the etching of the second conductive layer is performed until a top surface of the second conductive layer is at a lower level than a top surface of the first conductive spacers.

5. The method as claimed in claim 1, further comprising:

forming a first diffusion layer by implanting impurity ions into a portion of the substrate outside the trench, which is exposed by patterning the two-separated ONO dielectric layers;

forming second insulating spacers on exposed sidewalls of the patterned two-separated ONO dielectric layers and the first conductive spacers; and

forming a second diffusion layer by implanting impurity ions into the first diffusion layer using the second insulating spacers as an ion implantation mask.

6. The method as claimed in claim 5, wherein the second insulating spacers are formed of silicon oxide or silicon nitride using chemical vapor deposition or thermal oxidation.

7. The method as claimed in claim 5, further comprising performing a silicidation process for selectively forming a first silicide layer on the first conductive spacers and the second conductive layer for

connecting the first conductive spacers with the second conductive layer and selectively forming a second silicide layer on the second diffusion layer.

8. The method as claimed in claim 1, wherein the first conductive spacers and the second conductive layer are formed of conductive silicon.

9. A method of manufacturing a SONOS memory, the method comprising:

forming a silicon oxide-silicon nitride-silicon oxide (ONO) dielectric layer on a substrate;

forming a first conductive layer on the ONO dielectric layer;

forming a buffer layer on the first conductive layer, the buffer layer having a trench exposing a portion of the surface of the first conductive layer;

forming first insulating spacers on inner walls of the trench;

separating the first conductive layer and underlying ONO dielectric layer into two portions by sequentially removing the exposed portion of the first conductive layer and the ONO dielectric layer disposed thereunder using the first insulating spacers as an etch mask;

forming a gate dielectric layer on the exposed substrate resulting from the separation of the ONO dielectric layer, the gate dielectric layer extended onto exposed sidewalls of the separated first conductive layer and underlying ONO dielectric layer and the first insulating spacers inside the trench and also onto top surface of the buffer layer;

forming a second conductive layer on the gate dielectric layer to fill a gap between the inner walls of the trench;

removing the gate dielectric layer exposed by the second conductive layer;

removing the buffer layer using the first insulating spacers as an etch mask; and

patterning the two-separated first conductive layers and the underlying ONO dielectric layers by sequentially and selectively removing a

portion of each of the first conductive layer, which is exposed by removing the buffer layer, and a portion of each of the separated ONO dielectric layer disposed thereunder using the first insulating spacers as an etch mask.

10. The method as claimed in claim 9, wherein the gate dielectric layer is extended onto the first insulating spacers until the first insulating spacers are insulated from the second conductive layer to allow the second conductive layer and the two-separated and patterned first conductive layers to function as independent gates.

11. The method as claimed in claim 9, wherein forming the second conductive layer comprises:

depositing the second conductive layer on the gate dielectric layer to fill a gap between the inner walls of the trench completely; and

exposing a portion of the gate dielectric layer, which is extended onto the buffer layer by etching the second conductive layer using an etchback process or chemical mechanical polishing or both.

12. The method as claimed in claim 11, wherein the etching of the second conductive layer is performed until a top surface of the second conductive layer is at a lower level than a top surface of the first insulating spacers.

13. The method as claimed in claim 9, further comprising:

forming a first diffusion layer by implanting impurity ions into a portion of the substrate outside the trench, which is exposed by patterning the two-separated first conductive layers and the underlying ONO dielectric layers;

forming second insulating spacers on exposed sidewalls of the patterned two-separated ONO dielectric layers, the second insulating spacers extending onto exposed sidewalls of the first conductive layers and the first insulating spacers; and

forming a second diffusion layer by implanting impurity ions into the first diffusion layer using the second insulating spacers as an ion implantation mask.

14. The method as claimed in claim 13, further comprising performing a silicidation process for selectively forming a first silicide layer on the second conductive layer and selectively forming a second silicide layer on the second diffusion layer.

15. The method as claimed in claim 14, further comprising:

forming a capping insulating layer on the second conductive layer before removing the gate dielectric layer exposed by the second conductive layer; and

removing the capping insulating layer before performing the silicidation process.

16 The method as claimed in claim 13, wherein the first conductive layer and the second conductive layer are formed of conductive silicon.

17. The method as claimed in claim 15, wherein the capping insulating layer is formed by oxidizing a top surface of the second conductive layer formed of conductive silicon to a predetermined depth.

18. The method as claimed in claim 9, wherein the first insulating spacers are made of a material having etch selectivity with respect to the buffer layer.

19. A method of manufacturing a SONOS memory, the method comprising:

forming a silicon oxide-silicon nitride-silicon oxide (ONO) dielectric layer on a substrate;

forming a buffer layer on the ONO dielectric layer, the buffer layer having a trench exposing a portion of the surface of the ONO dielectric layer;

forming first insulating spacers on inner walls of the trench;

separating the ONO dielectric layer into two portions by selectively removing the exposed portion of the ONO dielectric layer using the first insulating spacers as an etch mask;

selectively removing the first insulating spacers;

exposing a portion of the silicon nitride layer by selectively removing upper silicon oxide layer of a portion of the separated ONO dielectric layer, which is exposed by removing the first insulating spacers;

forming a gate dielectric layer on the substrate, which is exposed by the separation of the ONO dielectric layer, the gate dielectric layer extended onto the silicon nitride layer and the buffer layer;

forming a conductive layer on the gate dielectric layer to fill a gap between the inner walls of the trench;

removing a portion of the gate dielectric layer, which is exposed by the conductive layer;

removing the buffer layer using the conductive layer as an etch mask; and

patterning the two-separated ONO dielectric layers by selectively removing a portion of the ONO dielectric layer, which is exposed by removing the buffer layer, using the conductive layer as an etch mask.

20. The method as claimed in claim 19, wherein the first insulating spacers are sacrificial layers formed of an insulating material other than the buffer layer or a photoresist material.

21. The method as claimed in claim 19, further comprising:

forming a first diffusion layer by implanting impurity ions into a portion of the substrate outside the trench, which is exposed by patterning the two-separated ONO dielectric layers;

forming second insulating spacers on the exposed sidewalls of the patterned two-separated ONO dielectric layers, the second insulating spacers extending onto an exposed sidewall of the gate dielectric layer surrounding the first conductive layer; and

forming a second diffusion layer by implanting impurity ions into the first diffusion layer using the second insulating spacers as an ion implantation mask.

22. The method as claimed in claim 19, wherein the gate dielectric layer is formed of silicon oxide using thermal oxidation or CVD.

23. The method as claimed in claim 19, wherein the conductive layer is formed of conductive silicon.

24. The method as claimed in claim 19, wherein forming the conductive layer comprises:

depositing the conductive layer on the gate dielectric layer to fill a gap between the inner walls of the trench completely; and

exposing a portion of the gate dielectric layer, which is extended onto the buffer layer by etching the conductive layer using an etchback process or chemical mechanical polishing or both.

25. A method of manufacturing a SONOS memory, the method comprising:

forming a first buffer layer on a substrate;

forming a second buffer layer on the first buffer layer, the second buffer layer having an etch selectivity with respect to the first buffer layer and including a trench exposing a portion of the surface of the first buffer layer;

removing the portion of the first buffer layer on a bottom part of the trench until the substrate disposed thereunder is exposed;

forming a silicon oxide-silicon nitride-silicon oxide (ONO) dielectric layer on the exposed substrate surface and inner walls of the trench;

forming first conductive spacers on the ONO dielectric layer formed on the inner walls of the trench;

separating the ONO dielectric layer into two portions by selectively removing the ONO dielectric layer using the first conductive spacers as an etch mask until the substrate disposed thereunder is exposed;

forming a gate dielectric layer on the exposed substrate resulting from the separation of the ONO dielectric layer, the gate dielectric layer extended onto exposed sidewalls of the first conductive spacers and top surface of the second buffer layer;

forming a second conductive layer on the gate dielectric layer to fill a gap between both sidewalls of the trench;

removing the gate dielectric layer exposed by the second conductive layer;

removing the second buffer layer using the first conductive spacers as an etch mask; and

patterning the two-separated dielectric layer by selectively removing a portion of the dielectric layer, which is exposed by removing the buffer layer, using the first conductive spacers as an etch mask.

26. The method as claimed in claim 25, wherein forming the second conductive layer comprises:

depositing the second conductive layer on the gate dielectric layer to fill a gap between inner walls of the trench completely; and

exposing a portion of the gate dielectric layer, which is extended onto the second buffer layer, by etching the second conductive layer using an etchback process or chemical mechanical polishing or both.

27. The method as claimed in claim 26, wherein the etching of the second conductive layer is performed until a top surface of the second conductive layer is at a lower level than a top surface of the first conductive spacers.

28. The method as claimed in claim 25, further comprising:

forming a first diffusion layer by implanting impurity ions into a portion of the substrate, which is exposed by patterning the ONO dielectric layer;

forming second insulating spacers on exposed sidewalls of patterned ONO dielectric layer, the second insulating spacers extending onto an exposed sidewall of the upper oxide layer of the ONO dielectric layer surrounding the first conductive spacers; and

forming a second diffusion layer by implanting impurity ions into the first diffusion layer using the second insulating spacers as an ion implantation mask.

29. The method as claimed in claim 25, further comprising performing a silicidation process for selectively forming a first silicide layer on the first conductive spacers and the second conductive layer for connecting the first conductive spacers with the second conductive layer and selectively forming a second silicide layer on the second diffusion layer.

30. The method as claimed in claim 25, wherein the first conductive spacers and the second conductive layer are formed of conductive silicon.

31. The method as claimed in claim 25, wherein the gate dielectric layer is formed of silicon oxide using thermal oxidation or CVD.

32. The method as claimed in claim 1, wherein the nitride layer in the ONO dielectric layer is any other insulating material having a charge trapping property.

33. The method as claimed in claim 9, wherein the nitride layer in the ONO dielectric layer is any other insulating material having a charge trapping property.

34. The method as claimed in claim 19, wherein the nitride layer in the ONO dielectric layer is any other insulating material having a charge trapping property.

35. The method as claimed in claim 25, wherein the nitride layer in the ONO dielectric layer is any other insulating material having a charge trapping property.